



Fig. 1

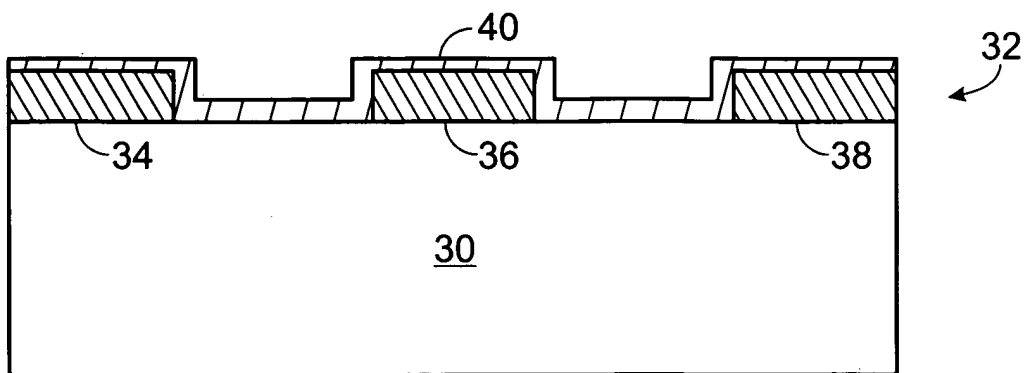


Fig. 2

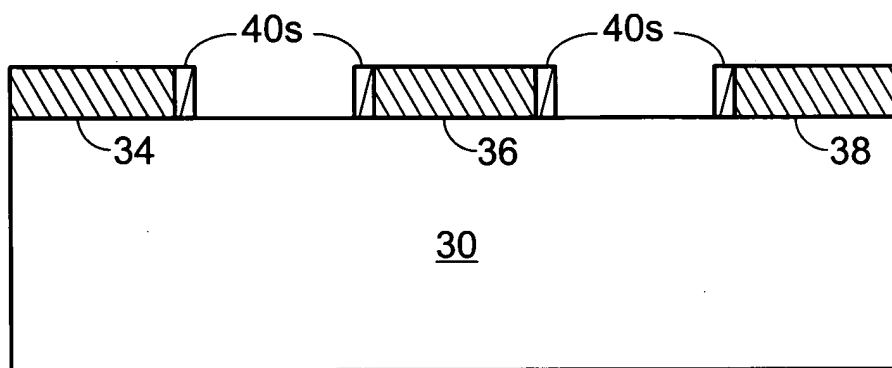


Fig. 3

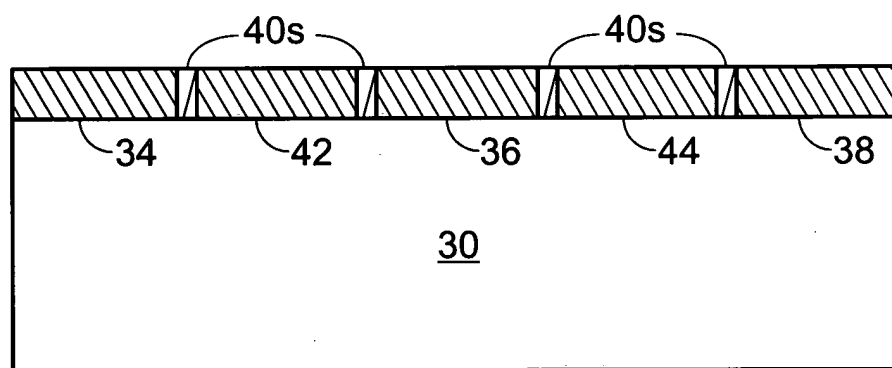


Fig. 4

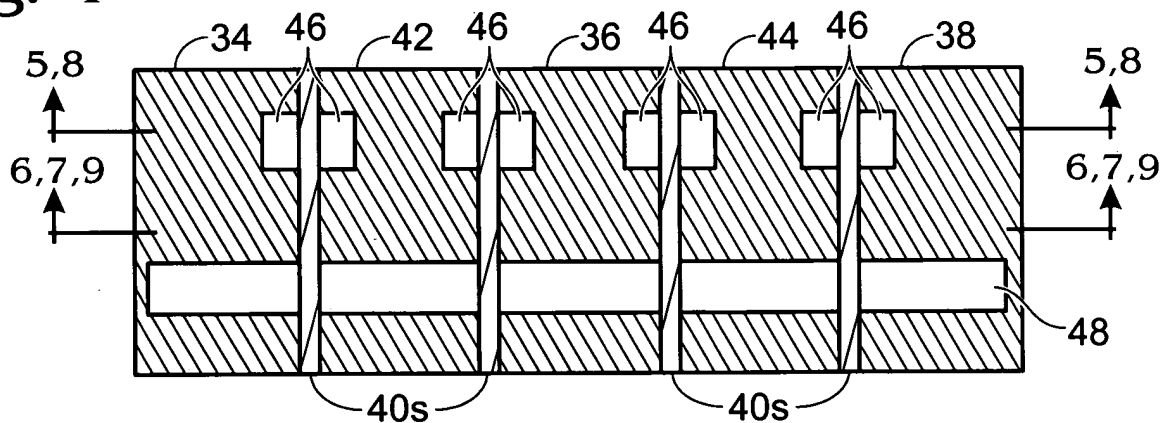




Fig. 5

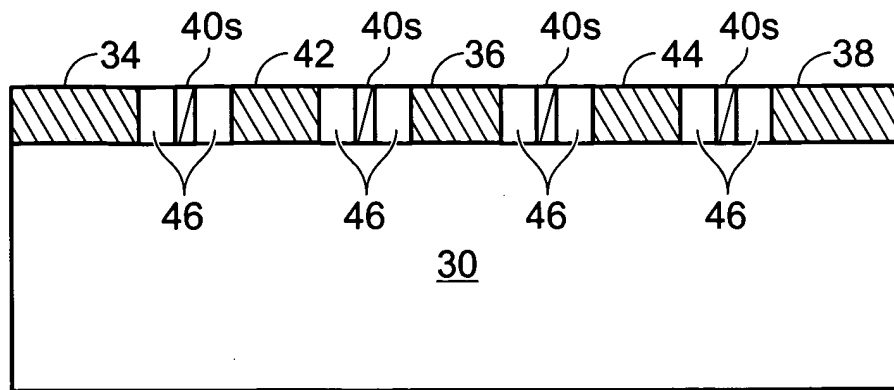


Fig. 6

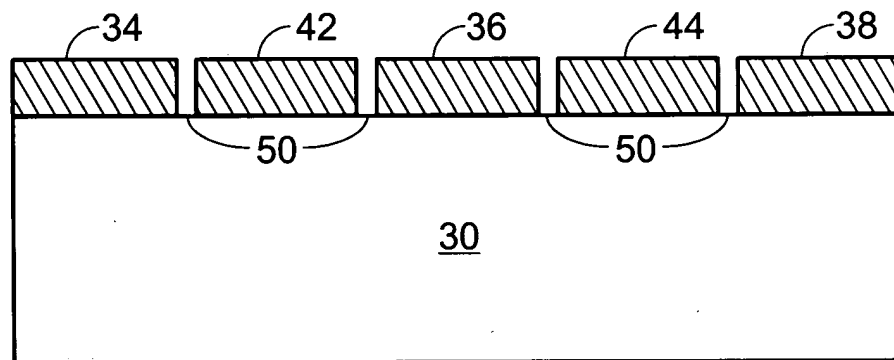


Fig. 7

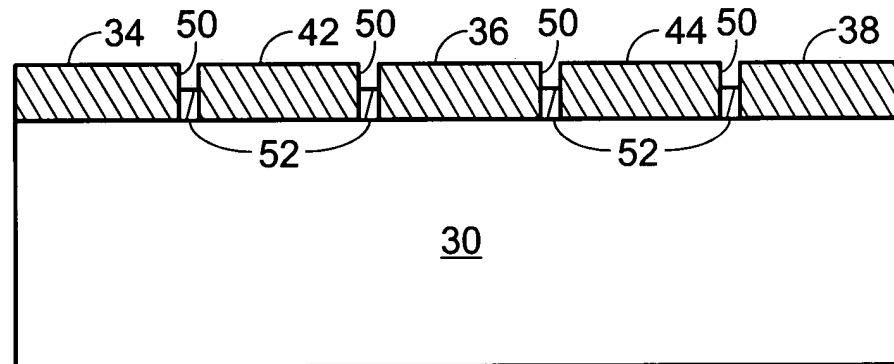


Fig. 8

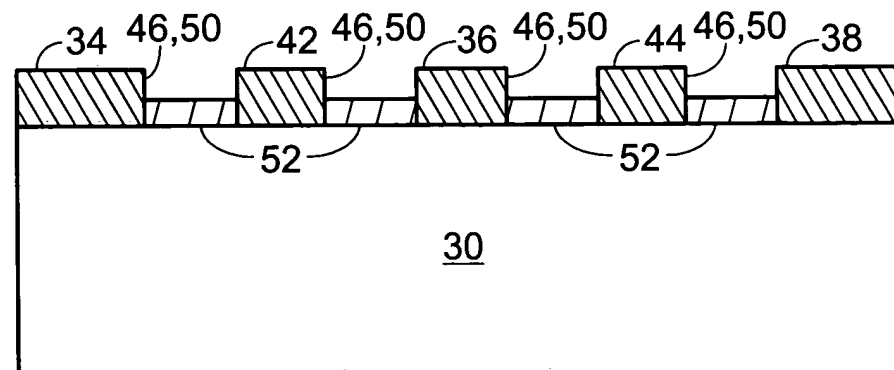




Fig. 9

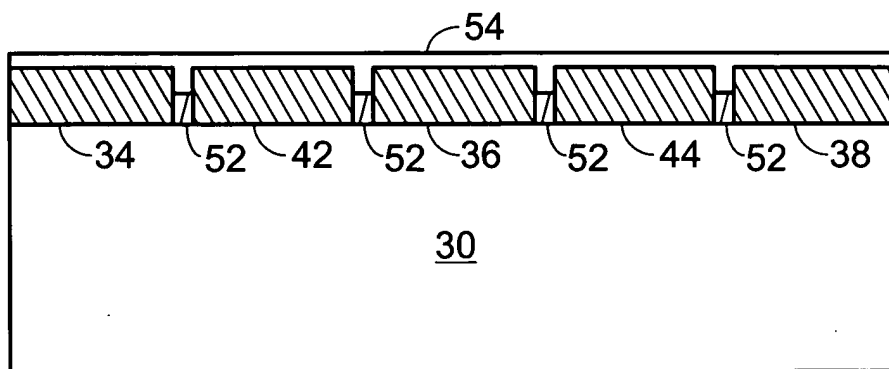


Fig. 10

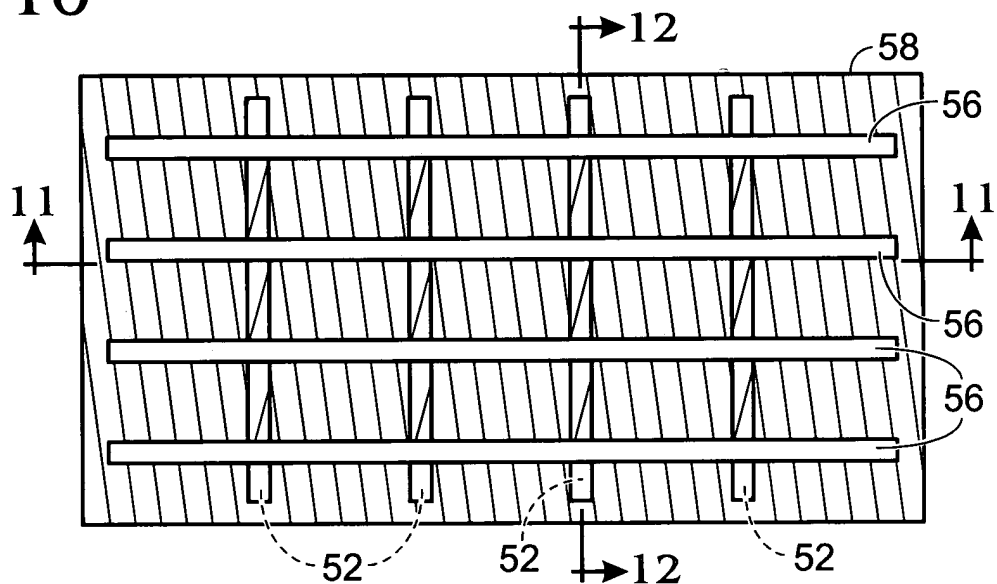
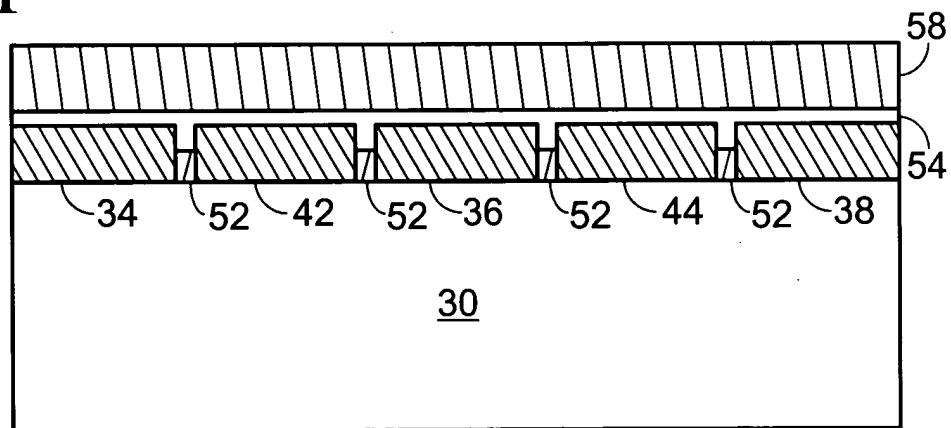


Fig. 11



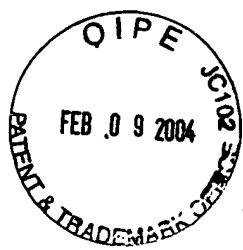


Fig. 12

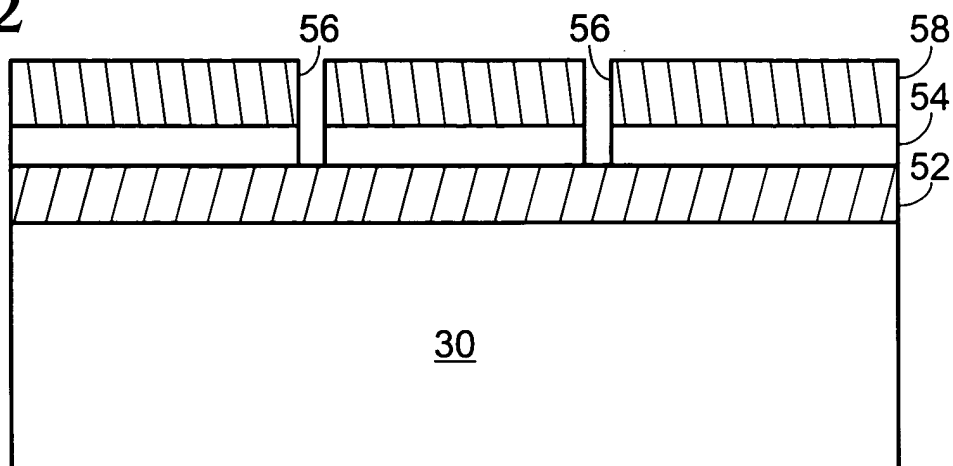


Fig. 13

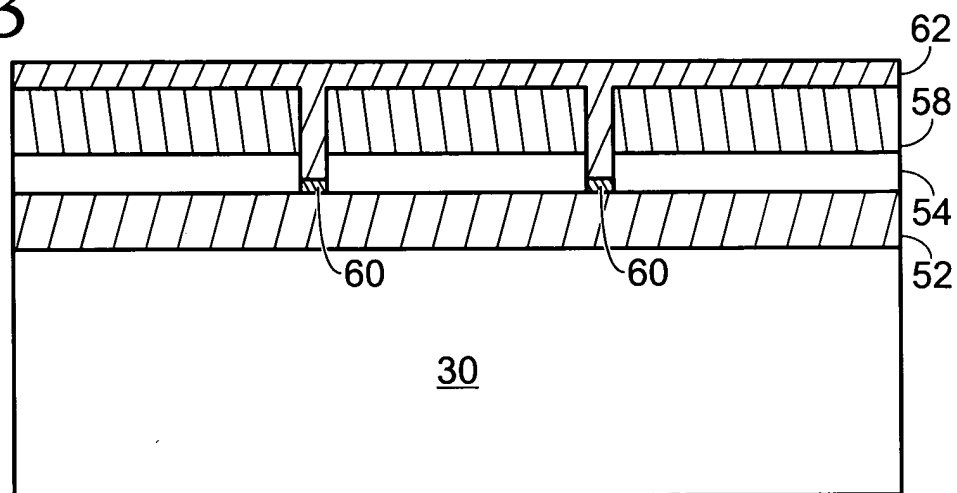


Fig. 14

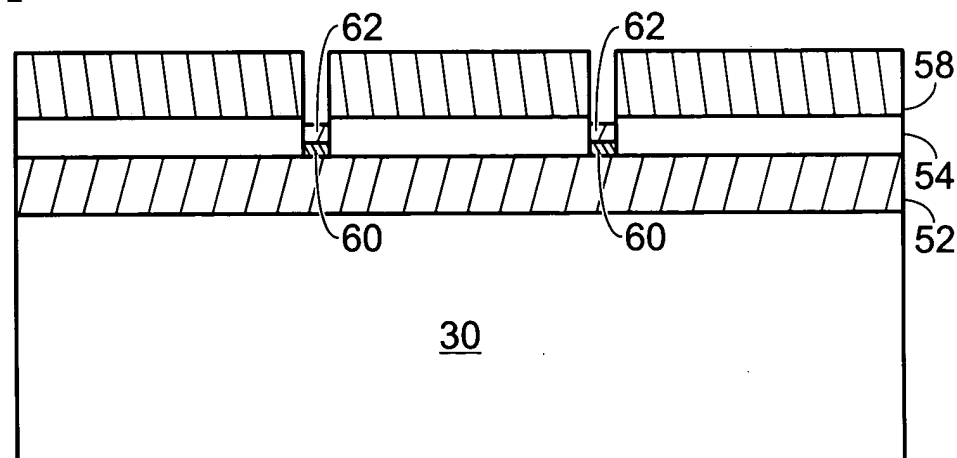




Fig. 15

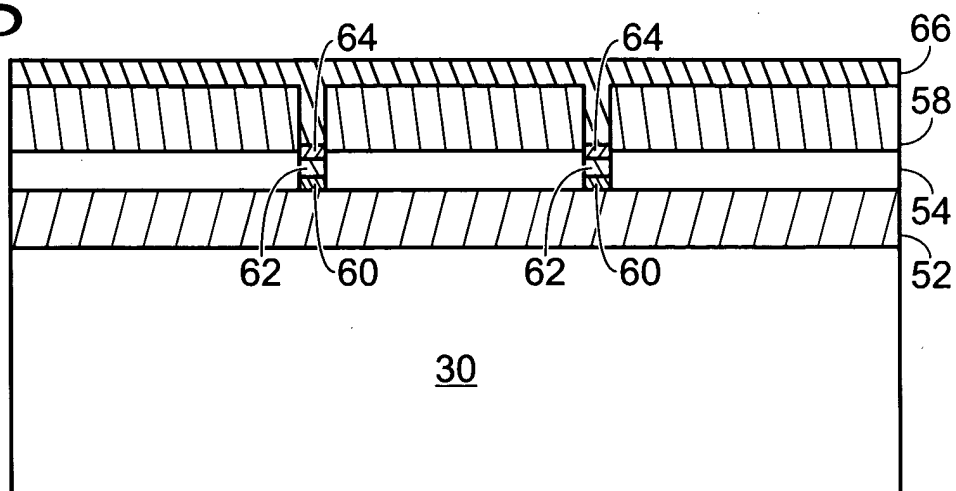


Fig. 16

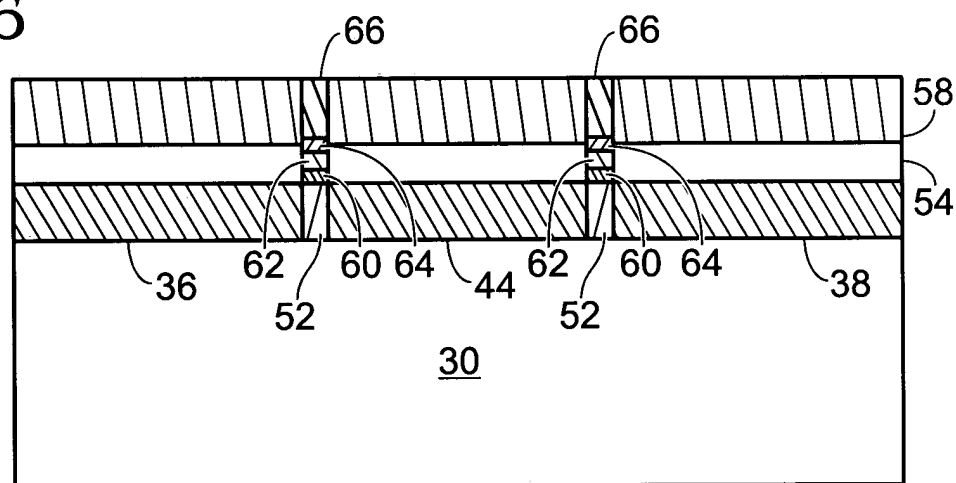


Fig. 17

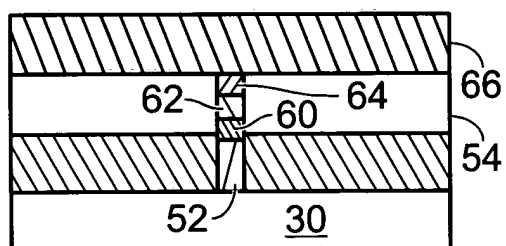


Fig. 18

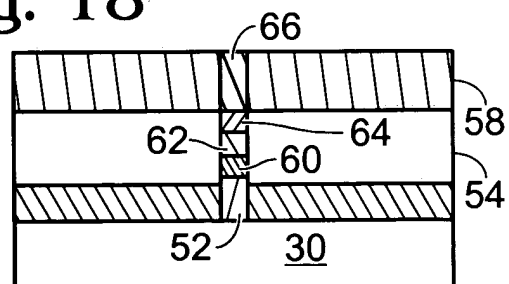




Fig. 19

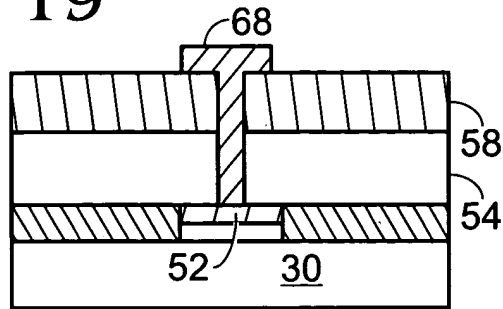


Fig. 20

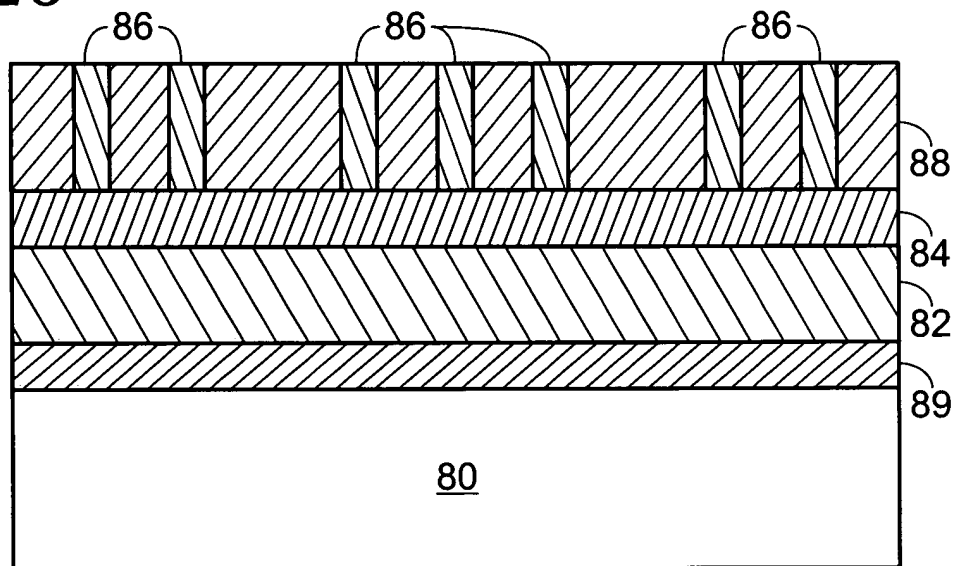


Fig. 21

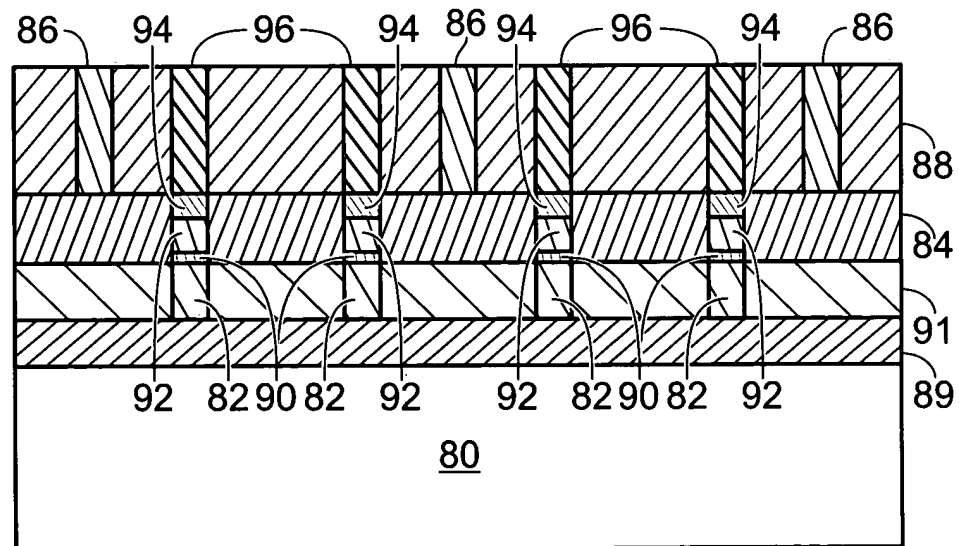




Fig. 22

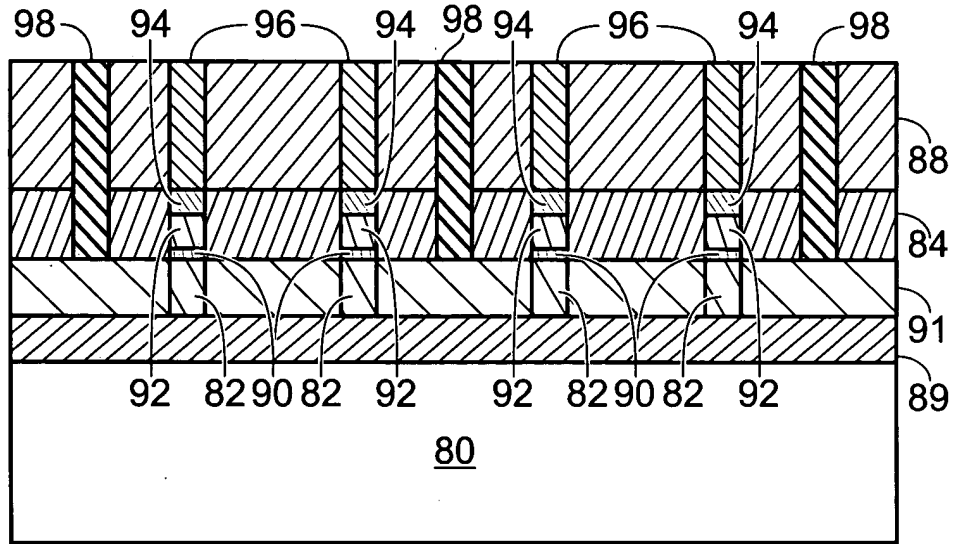
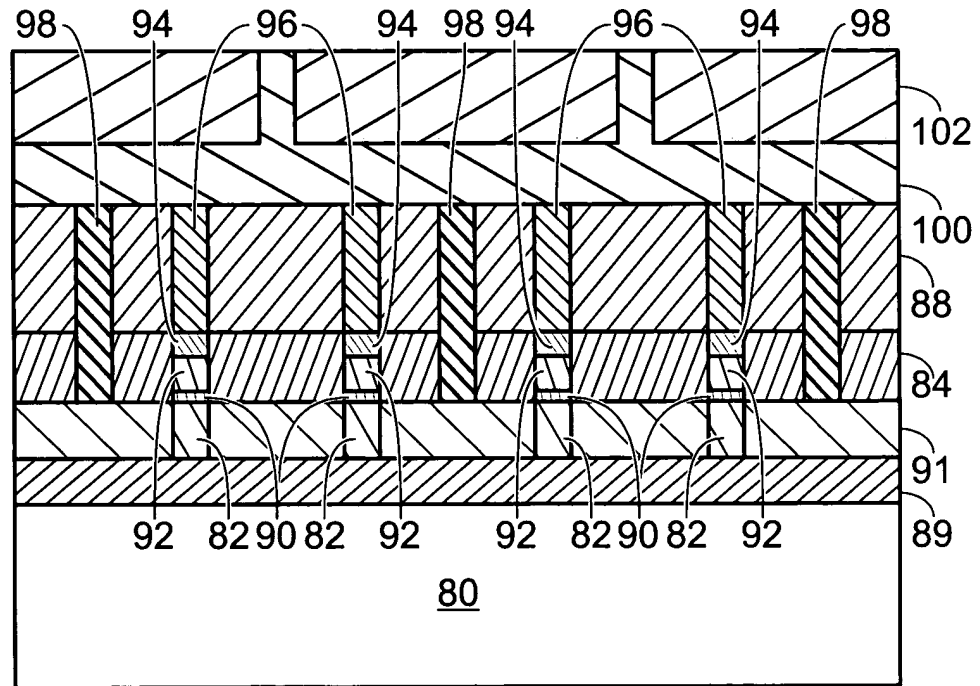


Fig. 23



This cross-sectional view shows a semiconductor device with a substrate 80. A bottom layer 89 is formed on the substrate. Above this, a layer 91 contains a series of rectangular openings. A layer 84 is deposited over the openings in layer 91. Within these openings, there are structures 82 and 90. A layer 88 is formed over the top of the structures 82 and 90. Above layer 88, there are regions 100 and 104. The topmost layer is 98. Various other regions and interfaces are labeled with numerals 92, 94, 96, and 98.

A cross-sectional view of a semiconductor device. The device consists of a substrate 80. On the substrate, there are repeating vertical structures. Each structure includes a vertical pillar 104. The pillars are separated by horizontal layers 84, 88, and 100. The pillars are also connected to a common horizontal layer 89. The pillars are connected to a common horizontal layer 91. The pillars are connected to a common horizontal layer 89. The pillars are connected to a common horizontal layer 91.